

# NbSi nanowire quantum-phase-slip circuits: dc supercurrent blockade, microwave measurements and thermal analysis

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We present a detailed report of microwave irradiation of ultra-narrow superconducting nanowires. In our nanofabricated circuits containing a superconducting NbSi nanowire, a dc blockade of current flow was observed at low temperatures below a critical voltage  $V_c$ , a strong indicator of the existence of quantum phase-slip (QPS) in the nanowire. We describe the results of applying microwaves to these samples, using a range of frequencies and both continuous-wave and pulsed drive, in order to search for dual Shapiro steps which would constitute an unambiguous demonstration of quantum phase-slip. We observed no steps, and our subsequent thermal analysis suggests that the electron temperature in the series CrO resistors was significantly elevated above the substrate temperature, resulting in sufficient Johnson noise to wash out the steps. To understand the system and inform future work, we have constructed a numerical model of the dynamics of the circuit for dc and ac bias (both continuous wave and pulsed drive signals) in the presence of Johnson noise. Using this model, we outline important design considerations for device and measurement parameters which should be used in any future experiment to enable the observation of dual Shapiro steps at experimentally accessible temperatures and thus lead to the development of a QPS-based quantum current standard.

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## I. INTRODUCTION

In recent years, there has been much interest in the phenomenon of quantum phase-slip (QPS) in ultra-narrow superconducting nanowires. This has been motivated by the potential applications for novel devices based on QPS including a charge-insensitive qubit<sup>1,2</sup> and a new quantum standard for electrical current.<sup>3</sup>

Research into other types of quantum current standard has also intensified following proposals to redefine several of the SI base units including the ampere.<sup>4</sup> The tunable barrier electron pump<sup>5</sup> is the front-runner amongst the competing technologies for realization of the ampere following redefinition in terms of a fixed value of the charge on the electron.<sup>6</sup> However, a quantum current standard based on quantum phase-slip in a superconducting nanowire is an attractive alternative, as it constitutes the exact dual of the Josephson voltage standard and therefore offers the potential for greater accuracy and scalability than the tunable barrier pump. In addition it would be a more elegant solution, being based on a truly quantum effect, and offers the future possibility of combining standards for current and voltage on a single chip.<sup>7,8</sup>

It is highly desirable to carry out a direct metrological triangle experiment in order to test the consistency of the present understanding that  $K_J = 2e/h$ ,  $R_K = h/e^2$  and  $q_c = 2e$ , where  $K_J$  is a constant characterizing the Josephson voltage standard,  $R_K$  is a constant obtained from the quantum Hall effect, and  $q_c$  is the charge transferred per cycle of the drive signal in our quantum current standard. This requires that the output from a quan-

tum current standard should be accurate to better than 1 part in  $10^7$  and that the magnitude of the current should exceed 100 pA to avoid an excessively long integration time.<sup>6,9,10</sup> The present state of the art in GaAs tunable barrier electron pumps is a current of magnitude 150 pA with an experimentally demonstrated current accuracy better than 1.2 parts per million and evidence based on modelling that the true accuracy approaches 1 part in  $10^8$ .<sup>5</sup>

A quantum current standard based on QPS arises from the exact duality between the Josephson junction and the quantum phase-slip junction (QPSJ).<sup>3,11</sup> This leads to the prediction that a QPSJ biased with a microwave signal should generate quantised current steps in its current-voltage ( $IV$ ) characteristic, dual to the quantised-voltage Shapiro steps observed in Josephson junctions which form the basis of the Josephson voltage standard. The QPSJ consists of an ultra-narrow superconducting nanowire in series with an inductance and a resistance sufficiently high for the single Cooper-pair regime to be reached<sup>3,11</sup> and overdamping of the circuit such that charge fluctuations are suppressed. The nanowire must have a sufficiently high normal-state resistivity and sufficiently small cross-sectional area to generate a sufficiently large QPS energy  $E_S \gg k_B T$  (dual to the Josephson energy  $E_J = (\Phi_0/2\pi)I_c$  where  $I_c$  is the critical current) and hence a sufficiently large critical voltage  $V_c = 2\pi E_S/2e$  to enable a clear observation of dual Shapiro steps.<sup>12</sup> Together with the constraint that the superconducting critical temperature  $T_c$  should be significantly higher than the lowest practical temperature achievable in a laboratory, this places restrictions

on the choice of material for the nanowire.

At present, NbSi and  $\text{InO}_x$  are considered to be the best candidates.<sup>2,13</sup> Ultra-narrow nanowires have been developed in both these materials with effective diameters in the range 20–40 nm.<sup>14–16</sup> QPS in  $\text{InO}_x$  has been demonstrated via spectroscopic measurements of  $E_S$  in a QPS qubit,<sup>2</sup> while alternative evidence for QPS (in fact, for the dual effect of coherent tunneling of single Cooper pairs) has been observed in NbSi nanowires via quantum interference in a device dual to the SQUID consisting of two QPSJs joined by a superconducting island.<sup>15</sup> Preliminary signs of QPS<sup>17,18</sup> and of dual Shapiro steps<sup>19</sup> have been observed in a Ti nanowire, but only traces of steps are observed.

In this article, we report dc and ac measurements of the  $IV$  curve of samples containing a NbSi nanowire embedded in a high impedance environment (*i.e.*, a single QPSJ). We present measurements on two samples, fabricated in the same facility as those reported in Ref. 15, and present representative results here. The dc measurements show a blockade of Cooper-pair transport along the nanowire, as expected with QPS; this is the dual of the blockade of phase motion (with, therefore, no developed voltage) in a Josephson junction for currents less than its critical current. The ac measurements were performed to search for evidence of dual Shapiro steps, predicted to occur at currents  $I = 2en\hbar f$ , where  $f$  is the ac frequency and  $n$  is an integer corresponding to the number of Cooper pairs transferred per cycle. Observation of these steps would constitute unambiguous demonstration of the QPS origin of the effect and rule out other explanations of the dc results, such as single-electron tunneling effects. However, no dual Shapiro steps were observed; instead, as the microwave power was increased, the blockade feature became less pronounced and increasingly rounded. These observations are consistent with heating of the sample. We describe thermal analysis and temperature-dependent measurements of the  $IV$  curve without microwave drive which indicate that the electron temperature in the circuit was elevated, resulting in Johnson noise sufficient to wash out any steps.

We also present a numerical model of the  $IV$  curve for dc and ac bias (both continuous wave and pulsed drive signals) in the presence of Johnson noise. We use this to predict an improved set of experimental parameters, comprising resistors of larger volume and higher resistivity and a pulsed drive signal with a higher pulse amplitude and lower pulse width, to enable the observation at experimentally accessible temperatures of dual Shapiro steps.

## II. FABRICATION AND CIRCUIT DESIGN

Figure 1 shows our superconducting nanowire sample and its environment. A NbSi nanowire of width 18–19 nm (*cf.* the estimated NbSi coherence length  $\approx 20$  nm<sup>15</sup>), length 5  $\mu\text{m}$  and thickness 10 nm was fabricated in se-

ries with a wider section of NbSi (width 25 nm, length 25.2  $\mu\text{m}$ ) which served as an additional kinetic inductance  $L_k$  exhibiting negligible QPS rate (since the QPS energy depends exponentially on the cross-sectional area of the wire,<sup>12</sup> a small increase in width results in a large decrease in QPS energy.) The nanowire and  $L_k$  line were embedded within a high-impedance environment comprising two CrO resistors each with design dimensions 70  $\mu\text{m} \times 80$  nm (width)  $\times$  10 nm (thickness). The NbSi and CrO components were connected via a AuPd micropad interface to ensure good adhesion and good electrical contact. AuPd was also used to fabricate the bond pads and an interdigitated capacitor (design value 50 fF) to enable ac biasing of the nanowire.

The chip was mounted on a chip carrier containing an SMA launcher and coplanar waveguide to transmit ac signals to the chip, as well as bond pads and leads to enable dc biasing. The waveguide was terminated with two 100  $\Omega$  resistors in parallel to provide a termination impedance of 50  $\Omega$ . A 2.2 pF capacitor was soldered between one of the dc leads and the ground plane to ensure a low-impedance path for ac signals to return to ground without passing through the current measurement path.

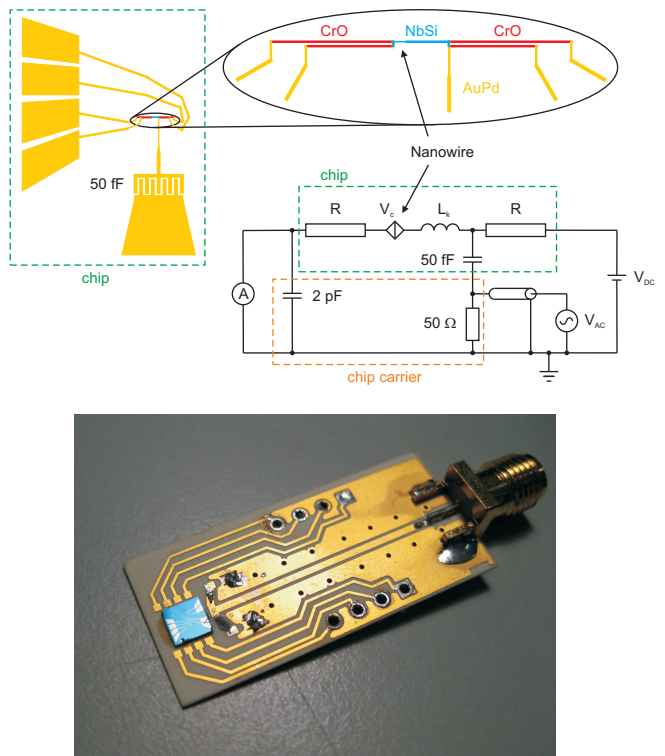


FIG. 1: Chip layout (not to scale) and circuit schematic. The photograph shows the chip mounted on the chip carrier. Note that the interdigitated capacitor and termination resistors are not present in the photograph.

The NbSi nanowire and the CrO resistors were fabricated by the same method as described in Ref. 15. The substrate was silicon with a 300 nm thermal-oxide

layer. First, the CrO resistors were fabricated together with AuPd contact wires and micropads in a single vacuum cycle utilizing shadow evaporation through a bilayer polymethyl methacrylate (PMMA) and copolymer stencil mask. The CrO resistors were evaporated at a low residual pressure of oxygen ( $\sim 10^{-6}$  mbar) followed by a 50 nm layer of AuPd from an angle for which the narrow stencil openings for the CrO resistors were overshadowed by the mask. This avoided the formation of AuPd shadows parallel to the CrO resistors. Next, the CrO resistors and other parts of the circuit were protected by a PMMA mask while a 10 nm film of amorphous  $\text{Nb}_x\text{Si}_{1-x}$  ( $x = 0.45$ ) was co-sputtered on the substrate, making contact only with the AuPd micropads. The value of  $x$  was defined by first calibrating the sputter rate for each element at a given sputter power and periodically confirmed by energy-dispersive x-ray (EDX) measurement using separately deposited films on Ge substrates. To remove organic residue and water before NbSi deposition, the micropads were cleaned by reactive ion etching with oxygen plasma and baking overnight in a  $\text{N}_2$  atmosphere at a temperature of 120°C. The substrate was rotated during deposition to ensure homogeneity of the film. After lift-off, the wafer was coated with inorganic negative-tone hydrogen silsesquioxane (HSQ) resist (XR-1541, Dow Corning) and patterned with an electron beam to define the nanowire and  $L_k$  line. Finally, the sample was etched with an inductively coupled plasma etching process with  $\text{SF}_6$  gas.

The sample contained four CrO resistors in total, two of length 70  $\mu\text{m}$  and two of length 50  $\mu\text{m}$  (see Fig. 1) to enable us to measure the resistance of the CrO resistors independently of the NbSi components. At room temperature, the resistance per unit length of the resistors was 9.25  $\text{k}\Omega \mu\text{m}^{-1}$  and a single CrO resistor of length 70  $\mu\text{m}$  had a resistance of 648  $\text{k}\Omega$ .<sup>39</sup>

The resistivity of the NbSi film was measured independently at  $T = 3.4$  K (above  $T_c \approx 1$  K)<sup>40</sup> and found to be  $\rho_N = 560 \mu\Omega\text{cm}$ .<sup>15</sup> Using the design dimensions of the nanowire and  $L_k$  line to calculate their normal state resistances we obtain 165  $\text{k}\Omega$  for the nanowire and 565  $\text{k}\Omega$  for the  $L_k$  line, yielding a total for the NbSi components of 730  $\text{k}\Omega$ , which agrees well with the measured value of 705  $\text{k}\Omega$ . We can estimate the kinetic inductance  $L_K$  of the NbSi components at  $T = 0$  using the formula<sup>20</sup>

$$L_K(0) = \frac{\hbar R_N}{\pi \Delta(0)} = 0.18 \frac{\hbar R_N}{k_B T_c}. \quad (1)$$

This yields  $L_K \approx 1000$  nH.

### III. DC MEASUREMENTS

We mounted the circuit shown in Fig. 1 in a dilution refrigerator and measured the  $IV$  characteristic under dc voltage bias. The dc lines were passed through feedthrough  $\pi$ -filters before entering the cryostat and

were subsequently filtered at 4 K and at base temperature. The filters at 4 K had an attenuation of  $\sim 90$  dB up to 2 GHz, dropping to  $\sim 30$  dB above 3 GHz. At base temperature, the copper powder filters had an attenuation of 30 dB at 40 MHz, rising to  $> 90$  dB above 100 MHz. The chip carrier was mounted within a copper enclosure on the tail of the dilution refrigerator which was bolted to the mixing chamber. dc voltage bias was provided by a source meter on the 20 V range, which had a noise floor of  $1 \mu\text{V Hz}^{-1/2}$  and a spike of amplitude  $55 \mu\text{V Hz}^{-1/2}$  at 50 Hz. We used a  $\times 10000$  divider to further reduce the noise amplitude. dc current was measured using a low-noise current pre-amplifier with a gain of  $10^8$  V/A, followed by a multimeter.

The measured  $IV$  characteristic is shown in Fig. 2. At the base temperature<sup>41</sup>, current blockade can be clearly seen. Controlling the power supplied to the still heater, the temperature dependence was measured. No change was observed between 33 mK (base temperature) and 100 mK. The increased rounding observed at the critical voltage is characteristic<sup>21</sup> of the effect of the Johnson noise generated in the CrO resistors.<sup>42</sup>

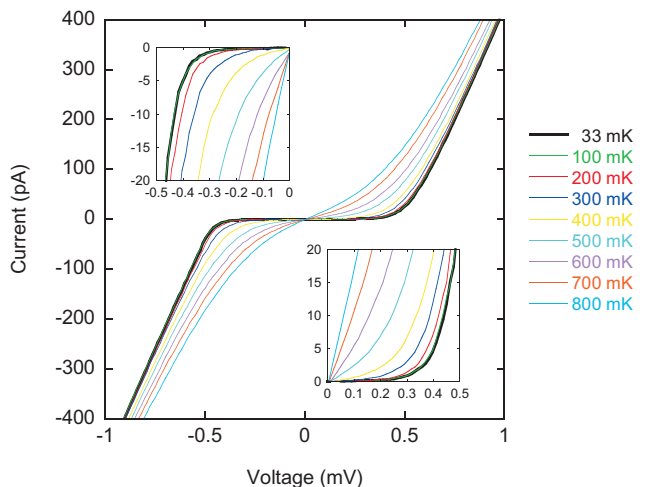


FIG. 2:  $IV$  characteristic of the NbSi nanowire embedded in its high-impedance environment. The thick dark line was measured at 33 mK. The coloured lines show measurements made at higher temperatures. The insets provide close-up views of the data.

At first glance, the  $IV$  characteristic appears to exhibit an excess voltage, i.e. the resistive branch, when extrapolated to zero voltage bias, intercepts the voltage axis at a non-zero value, which could be interpreted as being indicative of conventional Coulomb blockade due to single-electron tunneling.<sup>22</sup> However, as we show in Sec. V A, there is good qualitative agreement with numerical simulations of a QPS circuit, suggesting that, at higher bias voltage, the current would approach  $V/R$  as an asymptote. We have made measurements at higher voltages on other, nominally identical, samples which support this

view and measurements to higher bias on somewhat similar samples in Ref.<sup>15</sup> show no excess voltage. Further, Fig. 3 shows the inferred voltage drop across the superconducting nanowire (by subtracting the voltage drop  $IR$  across the CrO series resistors from the measured voltage). There is backbending in the transition to the resistive state, as expected for coherent single Cooper-pair tunneling.<sup>15,23</sup>

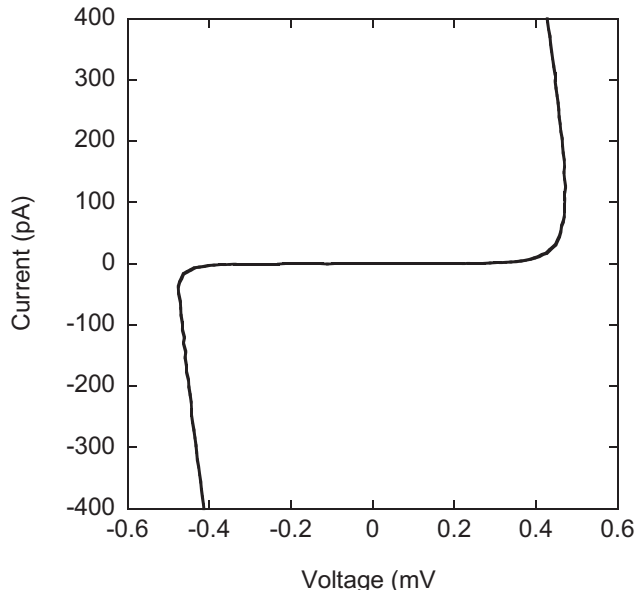


FIG. 3:  $IV$  characteristic at 33 mK with the voltage drop  $IR$  across the CrO resistors subtracted. backbending can be seen in the transition to the resistive branch, as expected in the presence of coherent single Cooper-pair tunneling (dual to the coherent QPS effect<sup>3,11</sup>).

#### IV. AC MEASUREMENTS WITH A CONTINUOUS-WAVE SIGNAL

In order to seek dual Shapiro steps as an unambiguous demonstration of the potential of the nanowire to exhibit QPS, we applied an additional continuous-wave ac voltage signal while sweeping the dc voltage bias. We applied ac signals at various frequencies and here present representative measurements at two frequencies, 100 MHz and 1.3 GHz. The ac signal was supplied by a high-power swept-signal generator, and a total of 55 dB of attenuation was included between the signal generator and the sample.<sup>43</sup> The ac voltage amplitude dropped across the  $50\ \Omega$  termination resistance on the chip carrier and, therefore, varied from 40 to 400  $\mu\text{V}$  rms as the total ac power varied from  $-75$  to  $-55$  dBm.

The measured  $IV$  characteristic at  $f = 100$  MHz is shown in Fig. 4. As the amplitude of the ac signal is increased, the blockade voltage becomes less pronounced

and more rounded until at  $-55$  dBm the curve is completely ohmic. No dual Shapiro steps were observed (expected at multiples of 32 pA at 100 MHz). The increased rounding of the curve with increasing ac amplitude is similar to the rounding caused by higher temperature (cf. Fig. 2) but, at higher bias, the current for a given bias voltage is much larger than expected due to heating; these features are similar to features expected in the presence of QPS, as we show in Sec. VB.

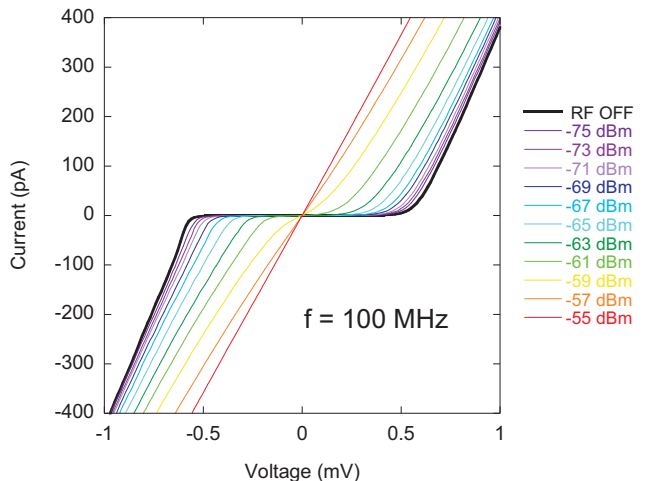


FIG. 4:  $IV$  characteristic under a continuous-wave ac bias of 100 MHz, measured at 33 mK. The thick dark line is the  $IV$  without the ac bias. The coloured lines show the gradual change that occurs as the amplitude of the ac signal is increased in steps of 2 dB from  $-75$  dBm (violet) to  $-55$  dBm (red).

In our case of large damping, at higher frequencies one expects dual Shapiro steps to have a larger maximum width  $V_n \approx 2(\omega/\omega_c)V_c = (4/2\pi)e\omega R$ , where  $\omega_c = 2\pi V_c/2eR$ ,<sup>24</sup> and, therefore, to be more robust against the effects of heating. However, when we applied an ac signal at a higher frequency of 1.3 GHz, we once again observed no dual Shapiro steps (these would be expected at multiples of 420 pA at 1.3 GHz). Figure 5 shows the measured  $IV$  characteristic at 1.3 GHz, applied to a different sample with the same nominal design. Increased noise present in these data (compared to that obtained at 100 MHz) is due to the use of a different current preamplifier and a lower divider of  $\times 10$  on the output of the voltage source. The transition to the resistive state once again becomes more rounded at higher amplitudes, consistent with significant heating.

The observed blockade voltage in this sample was lower (around 250  $\mu\text{V}$ ), although the nanowire dimensions were nominally virtually identical. This critical-voltage  $V_c$  variation between samples is likely to be associated with small inhomogeneities in the cross section of the wires which result in areas of locally increased resistance where the QPS rate is enhanced so the value of  $V_c$  depends on the number, strength and relative phases of these

spots.<sup>15,25</sup> We note that it was argued in Ref. 15 that the behavior of a sufficiently short wire containing several weak segments at different positions is similar to that of a single QPS junction having equivalent energy  $E_S$  equal to a (vector) sum of individual QPS energies. This sum is maximised when the electric polarization of sections of nanowire between the weak segments is uniform (or zero), corresponding to equal phases for the individual QPS segments.

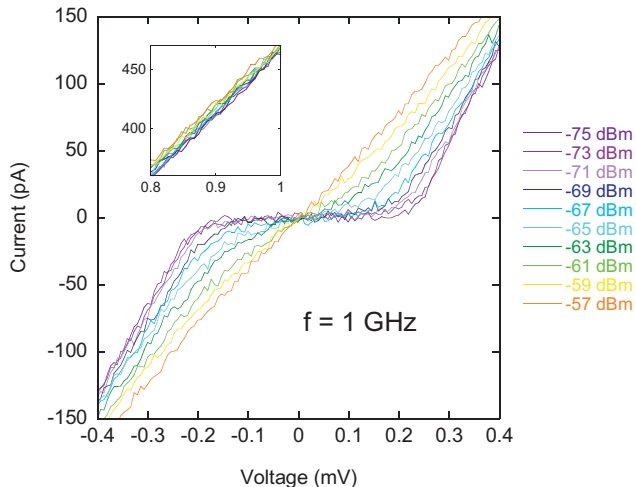


FIG. 5:  $IV$  characteristic under a continuous-wave ac bias of 1.3 GHz, measured at 33 mK for increasing ac amplitudes. The inset shows the region in which a dual Shapiro step would be expected (420 pA). The increased noise present in these data, compared to that obtained at 100 MHz, is due to the use of a different current preamplifier and a lower divider of  $\times 10$  on the output of the voltage source.

## V. NUMERICAL MODEL OF THE $IV$ CHARACTERISTIC OF A QPSJ

In order to better understand the effect of an elevated electron temperature on the  $IV$  characteristic of a QPSJ, we have constructed a numerical model for the circuit dynamics which includes a temperature-dependent Johnson noise term and in this section we present simulations of the system at a number of different temperatures.

A QPSJ consisting of a superconducting nanowire in series with an inductance and a resistance (see Fig. 6) is the exact dual of a Josephson junction shunted by a capacitor and a resistor (RCSJ).<sup>3</sup> Therefore, a QPSJ can be modelled using an equation of motion exactly dual to that of the RCSJ model:

$$V(t) = V_c \sin\left(\frac{2\pi q}{2e}\right) + L_K \frac{d^2 q}{dt^2} + R \frac{dq}{dt} + V_n, \quad (2)$$

where  $V(t)$  is the applied voltage bias (dc or a combination of dc and ac),  $q$  is the total charge to pass through

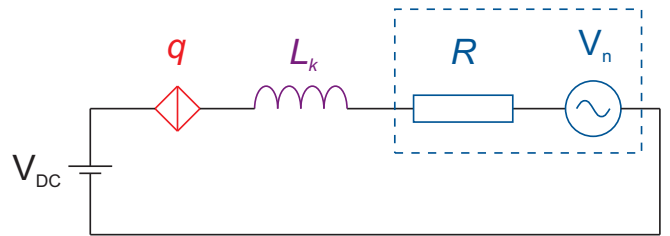


FIG. 6: Equivalent circuit of a quantum phase-slip junction. The resistance  $R$  includes both CrO resistors. Johnson noise is included by modelling the resistance as an ideal voltage source with output resistance  $R$  and a random, Gaussian signal as a function of time.

the nanowire since time  $t = 0$ ,  $e$  is the charge on an electron,  $V_c$  is the critical voltage of the nanowire,  $L_K$  is the combined kinetic inductance of the nanowire and the wider  $L_K$  line,  $R$  is the combined resistance of the CrO resistors, and the Johnson-noise voltage generated by  $R$  is given by

$$V_{n,\text{rms}} = \sqrt{4k_B R T B}, \quad (3)$$

where  $k_B$  is Boltzmann's constant,  $T$  is the electron temperature and  $B$  is the bandwidth of the circuit.

We used a fourth-order Runge-Kutta technique, with a Gaussian-distributed random-number generator for  $V_n(t)$ , to solve this equation for a series of dc voltage bias points  $V_{\text{bias}}$ , yielding oscillatory solutions for  $q(t)$  and  $I(t) = dq/dt$ . By averaging  $I(t)$  over many cycles, we obtained a value for the dc current corresponding to each dc voltage bias point, and thus obtained simulations of the  $IV$  characteristic. None of our simulated  $IV$  curves is completely smooth, due to the finite number of points over which the dc current was averaged.

### A. dc simulations

For a dc voltage bias, the drive term in Eq. 2 is simply  $V(t) = V_{\text{bias}}$ . In order to understand the effect of an elevated electron temperature on the dc  $IV$  curve, we choose simulation parameters that give good qualitative agreement with the data shown in Fig. 2:  $V_c = 700 \mu\text{V}$ ,  $L_K = 890 \text{ nH}$  and  $R = 1.6 \text{ M}\Omega$ . These are close to the design values for the measured circuit:  $L_K = 1000 \text{ nH}$  and  $R = 1.3 \text{ M}\Omega$ . We find that the shape of the  $IV$  curve is rather insensitive to the value chosen for  $L_K$ , because the simulation parameters lie in the strongly damped regime with a  $Q$ -value of 0.069.<sup>44</sup> The bandwidth of the circuit below  $V_c$  is limited by the cut-off frequency,  $\omega_c = 1/RC_{\text{QPS},0} \approx 8 \times 10^9 \text{ s}^{-1}$ , where  $C_{\text{QPS},0} = 2e/(2\pi V_c)$  is the (zero-voltage) QPS nonlinear capacitance analogous to the (zero-current) Josephson inductance  $L_J = \Phi_0/(2\pi I_c)$ .<sup>45</sup> The bandwidth varies as a function of voltage bias below  $V_c$ , decreasing as the bias voltage increases towards  $V_c$ , due to the increase of the



capacitance to  $C_{\text{QPS}} = C_{\text{QPS},0} / \cos(\arcsin V/V_c)$ . Above  $V_c$  the bandwidth is limited by the roll-off frequency of the series resistors, which become capacitive at high frequencies. For our simulations, for simplicity, we chose a fixed bandwidth of 18 GHz, similar to the roll-off frequency of the CrO resistors.<sup>26</sup>

Fig. 7 shows simulations of the dc  $IV$  characteristic at temperatures corresponding to those for which the curve was measured experimentally. The simulations are qualitatively similar to the measured curves shown in Fig. 2, with the best agreement obtained at the highest temperatures. There are differences in some details. For example, at lower temperatures, the differential conductance in the simulations first increases with increasing  $V$  bias and then above some voltage  $V \lesssim V_c$  decreases as  $V$  bias is further increased, whereas in the experimental data the differential conductance is increasing as  $V$  bias increases from zero up to the highest bias at which we measured. This difference appears not to be associated with heating and is likely to relate to details of the experimental circuit not included in the model for the simulations. One possible reason for the behaviour could be frequency dependence of the resistor impedance associated with its parasitic capacitance.

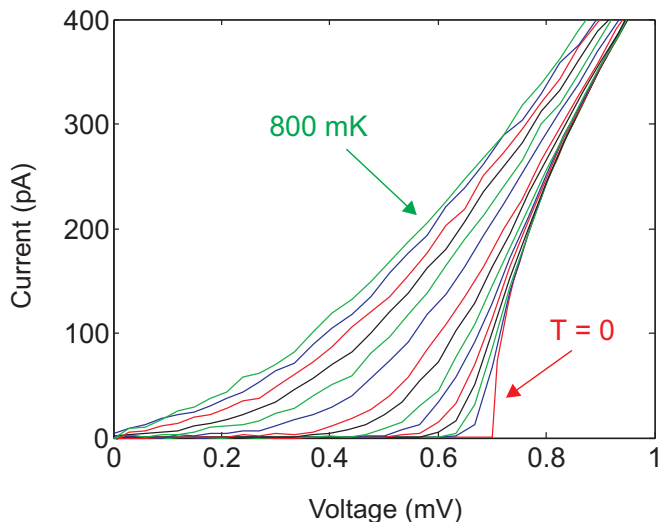


FIG. 7: Simulated  $IV$  characteristic at temperatures 0 K, 10 mK, 20 mK, 33 mK, 50 mK, 75 mK, 100 mK, 150 mK, 200 mK, 300 mK, 400 mK, 500 mK, 600 mK, 700 mK and 800 mK. The ripples in the curves are due to the finite number of points over which the dc current was averaged.

Fig. 8 compares the simulations with the data, showing good qualitative agreement between data and simulation at 800 mK. The data taken at 33 mK (the base temperature of the dilution refrigerator) agree best with a simulation at 150 mK, suggesting an elevated electron temperature.

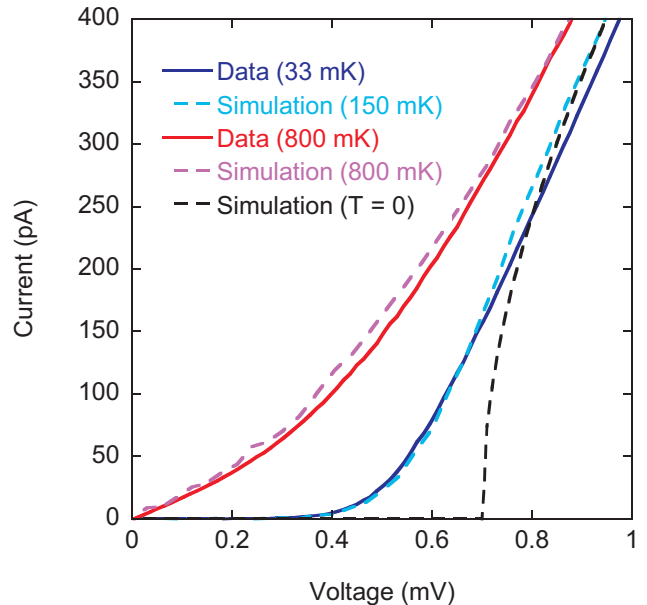


FIG. 8: Comparison of simulated  $IV$  characteristics with data taken at 33 mK and 800 mK.

## B. Continuous-wave ac simulations

To model the behaviour in the presence of an ac bias signal, we consider a circuit in which the ac and dc bias voltages are combined via a bias tee before being applied to the QPSJ circuit including both CrO resistors (Fig. 9). The drive term in Eq. 2 then becomes  $V(t) = V_{\text{bias}} + V_{\text{ac}} \sin \omega t$ , where  $V_{\text{ac}}$  is the amplitude and  $\omega = 2\pi f$  is the angular frequency of the ac signal. This circuit is slightly simpler than the actual circuit shown in Fig. 1, where the ac currents passing through the two CrO resistors differ.

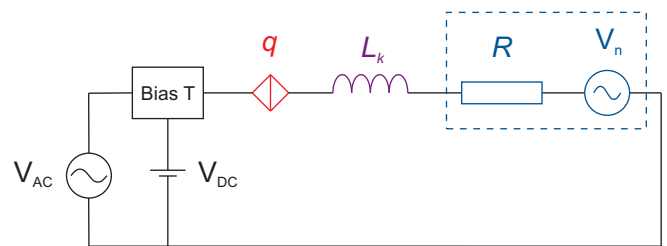


FIG. 9: Quantum phase-slip junction with combined dc and continuous-wave ac voltage bias. The resistance  $R$  includes the resistance of both CrO resistors.

Figure 10 shows the simulation results for a continuous-wave ac signal of frequency 100 MHz and amplitude  $V_{\text{ac}}$  ranging from 40 to 250  $\mu\text{V}$ .<sup>46</sup> At  $T = 0$ , the simulations exhibit dual Shapiro steps at multiples of 32 pA. At higher  $T$ , thermal fluctuations wash out the steps and, for temperatures of 200 mK and higher, the features arising in the simulation also arise in a crude rectification

model (not shown) in which the dc current is obtained from the observed dc  $IV$  curve by a simple average over an ac cycle of the currents corresponding to the instantaneous ac voltages. At 33 mK, some departure from the crude rectification model due to the nonlinearity in Eq. 2 is still visible. Comparison with cw experimental measurements in Fig. 4 shows good qualitative agreement and suggests that the electron temperature in the lowest- $T$  cw measurements lies below 200 mK.

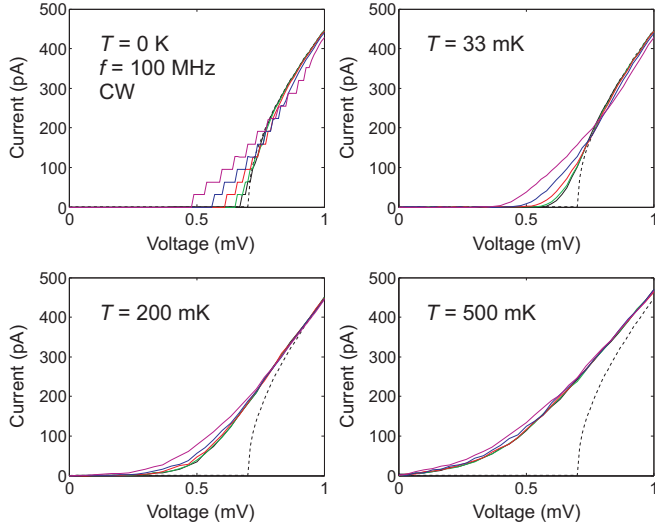


FIG. 10: Simulated  $IV$  characteristics at  $T = 0$  K, 33 mK, 200 mK and 500 mK for a continuous-wave ac signal of frequency 100 MHz and amplitude  $40 \mu\text{V}$  (black),  $63 \mu\text{V}$  (green),  $100 \mu\text{V}$  (red),  $160 \mu\text{V}$  (blue) and  $250 \mu\text{V}$  (purple). The ripples in the curves are due to the finite number of points over which the dc current was averaged. The  $IV$  curve at  $T = 0$  in the absence of an ac signal is shown as a black dashed line.

In Fig. 11, we show simulations performed at a higher frequency of 1 GHz, keeping the other simulation parameters the same as those used at 100 MHz. At  $T = 0$ , a single dual Shapiro step appears at a current of 320 pA and becomes broader as  $V_{ac}$  increases. At  $T = 33$  mK, the step can still be observed, although it is somewhat rounded by thermal fluctuations. At  $T = 200$  mK and higher, the step is washed out.

### C. Pulsed simulations

In the last section we showed that increases in the frequency and amplitude of the ac signal can be made in order to increase the width of steps and that this increases the likelihood of observing steps at higher temperatures. In this section, we show that the step width can be further increased by applying a pulsed signal, rather than a continuous-wave signal<sup>27–29</sup> and once again consider the circuit shown in Fig. 9. The drive term  $V(t)$  now consists of a series of pulses of amplitude  $V_{ac}$ , width  $w_p$  and repetition rate  $\omega/2\pi$ , added to the dc voltage bias  $V_{bias}$ .

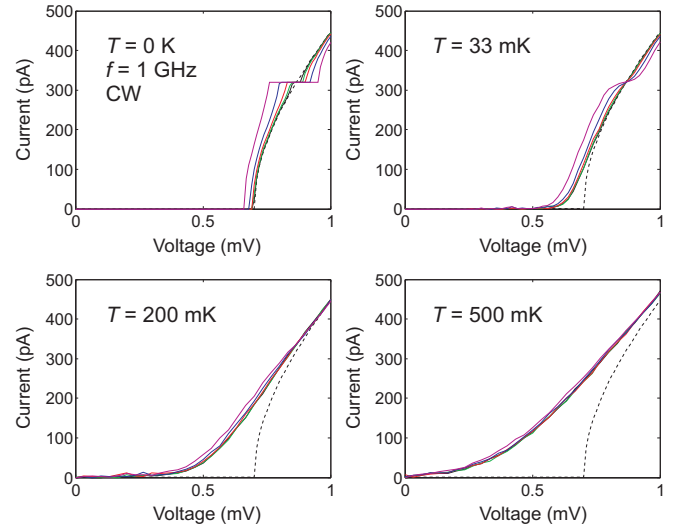


FIG. 11: Simulated  $IV$  characteristics at  $T = 0$  K, 33 mK, 200 mK and 500 mK for a continuous-wave ac signal of frequency 1 GHz and amplitude  $40 \mu\text{V}$  (black),  $63 \mu\text{V}$  (green),  $100 \mu\text{V}$  (red),  $160 \mu\text{V}$  (blue) and  $250 \mu\text{V}$  (purple), applied in series with the dc voltage bias. The  $IV$  curve at  $T = 0$  in the absence of an ac signal is shown as a black dashed line.

Simulations at a pulse repetition rate  $f$  of 100 MHz and pulse width 3 ns are shown in Fig. 12 for a variety of pulse amplitudes, keeping the other simulation parameters the same as for the continuous-wave simulations. The first-order dual Shapiro step is expected at  $2ef \approx 32$  pA. At  $T = 0$ , there are many small dual Shapiro steps, including noninteger steps due to higher-order processes. At 33 mK, the integer steps are still visible at the highest pulse amplitudes, although somewhat rounded. At 200 mK and above, the steps are washed out. Compared to the simulations at 100 MHz using a continuous-wave signal, the steps are observable at a higher temperature.

Simulations at a higher pulse repetition rate of 1 GHz and a smaller pulse width of 0.1 ns are shown in Fig. 13. These show a broad dual Shapiro step at  $T = 0$ , the width of which increases with increasing pulse amplitude. At 33 mK, the step is still visible and exhibits a significant plateau region at the highest pulse amplitudes, despite the rounding due to thermal fluctuations. At 200 mK, the step is still just visible at the highest pulse amplitudes, although it is washed out at 500 mK.

Therefore, by using a pulsed signal, the step can be made much broader than for a continuous-wave signal of comparable amplitude. At 33 mK (the base temperature of our dilution refrigerator), the step exhibits a plateau of suitable breadth and at a suitable current ( $> 100$  pA) for a prototype quantum current standard.

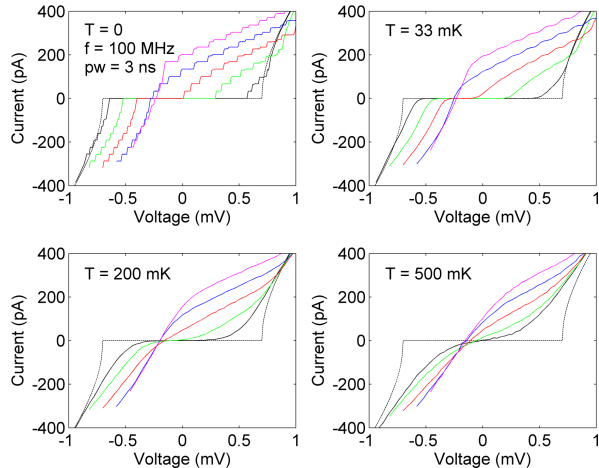


FIG. 12: Simulated  $IV$  characteristics at  $T = 0$  K, 33 mK, 200 mK and 500 mK for a pulsed ac signal with pulse width 3 ns, pulse repetition rate 100 MHz and amplitude 200  $\mu$ V (black), 600  $\mu$ V (green), 1 mV (red), 1.4 mV (blue) and 1.8 mV (purple), applied in series with the dc voltage bias. The  $IV$  curve at  $T = 0$  in the absence of a pulsed signal is shown as a black dashed line.

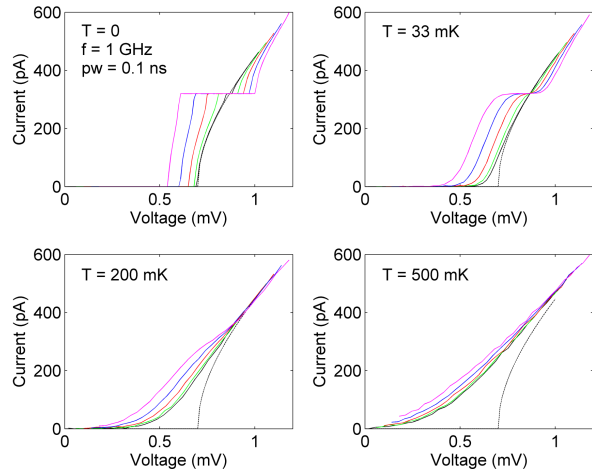


FIG. 13: Simulated  $IV$  characteristics at  $T = 0$  K, 33 mK, 200 mK and 500 mK for a pulsed ac signal with pulse width 0.1 ns, pulse repetition rate 1 GHz and amplitude 200  $\mu$ V (black), 600  $\mu$ V (green), 1 mV (red), 1.4 mV (blue) and 1.8 mV (purple), applied in series with the dc voltage bias. The  $IV$  curve at  $T = 0$  in the absence of a pulsed signal is shown as a black dashed line.

## VI. MEASUREMENTS WITH A PULSED SIGNAL

Since the numerical modeling predicts broader steps for a pulsed drive than for a continuous-wave ac drive, we

carried out measurements of the  $IV$  curve while applying a pulsed signal in addition to the dc bias voltage.

Using the same sample as for the continuous-wave ac measurements at 100 MHz, we applied a pulsed signal with repetition rate 100 MHz and pulse width 3 ns (respectively, the upper frequency limit and lower pulse-width limit possible with our pulse generator). Figure 14 shows the measured  $IV$  characteristic. The pulse amplitude at the source ranged from  $-500$  mV to  $+500$  mV, corresponding to a range of  $-2$  to  $+2$  mV across the 50  $\Omega$  termination resistance on the chip carrier.

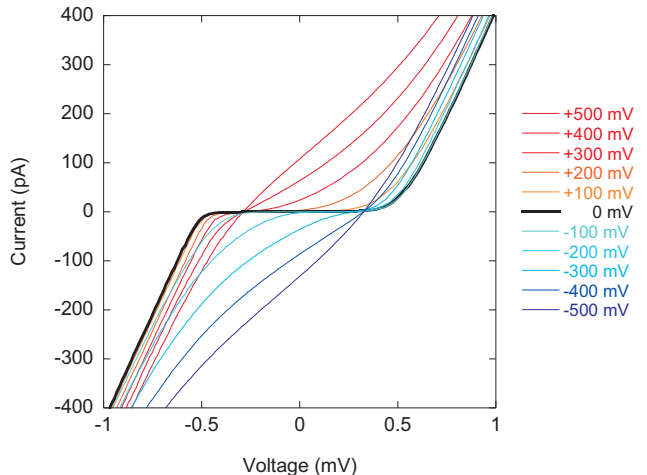


FIG. 14: Measured  $IV$  characteristic using a pulsed drive with a pulse repetition rate of 100 MHz and pulse width 3 ns, measured at 33 mK. The thick dark line is the  $IV$  curve at a pulse amplitude of 0 V. The coloured lines are for pulse amplitudes increasing in steps of 100 mV in the negative (blue) and positive (red) directions. The curve at zero amplitude is not identical to the  $IV$  characteristic when the pulse generator was switched off, suggesting that some power was being emitted even when the generator was set to zero amplitude.

The  $IV$  characteristic is not symmetric about the origin, due to the asymmetric nature of the pulsed signal. No dual Shapiro steps are visible. Indeed we experimentally probed the  $IV$  characteristic over a range of pulse repetition rates from 10 to 100 MHz and a range of pulse widths from 3 to 10 ns, but did not observe dual Shapiro steps with any combination of parameters.

The pulsed experimental data (taken at the base temperature of 33 mK) shows qualitative similarities to the pulsed simulations at 100 MHz at 200 and 500 mK (see Fig. 12) which supports the view that the electron temperature was elevated above the base temperature of the dilution refrigerator. In the following section we present a more quantitative evaluation of the influence of heating on the circuit.



## VII. THERMAL ANALYSIS

Comparison of the measurements and simulations presented in the previous sections point to heating in the circuit washing out any dual Shapiro steps. Therefore, in this section, we present a simple lumped-element model of the thermal properties of the QPSJ circuit. We use this to evaluate the thermal time constants of the system and to calculate the equilibrium electron temperature in the CrO resistors. Evaluation of the electron temperature allows us to consider modifications that can be made to the dimensions and materials of the resistive elements to reduce the effect of heating. Evaluation of the time constants allows us to consider the benefit of pulsed measurements in mitigating heating.

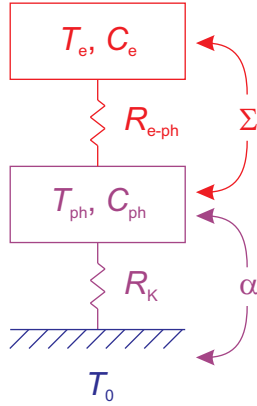


FIG. 15: Lumped-element model for heat flow from a resistor to the SiO<sub>2</sub> substrate.

Our lumped-element model for heat flow in a resistor is shown in Fig. 15. As current is passed through the resistor, power  $P = I^2 R$  is dissipated, causing the electron temperature  $T_e$  to rise via Joule heating. Heat flows from the electron sea to the lattice via the thermal resistance  $R_{e-ph}$  and then from the lattice to the substrate via the Kapitza thermal boundary resistance  $R_{Kapitza}$ . Other relevant material parameters for the model are  $C_e$  and  $C_{ph}$ , the electronic and phonon specific heat capacities, respectively,  $\Sigma$  is the electron-phonon coupling constant and  $\alpha$  is the thermal coupling constant across the boundary between the resistor and the substrate. In what follows, we denote the lattice temperature  $T_{ph}$  and the temperature of the SiO<sub>2</sub> substrate, which acts as a cold reservoir,  $T_0$ .

### A. Thermal time constants

We first consider the response of the system to a change in current. The electron and lattice temperatures change with time constants  $\tau_1 = R_{e-ph} C_e (N_e/N_A)$  and  $\tau_2 = R_K C_{ph} (N_c/N_A)$  respectively, where  $N_A$  is Avogadro's constant,  $N_e$  is the total number of electrons in the resistor and  $N_c$  is the number of primitive cells in

the lattice. In the free-electron model,  $C_e$  is given by  $C_e = \gamma T_e$ , where

$$\gamma = \frac{\pi^2 N_A k_B}{2 T_F}, \quad (4)$$

and  $T_F$  is the Fermi temperature.<sup>30</sup> The electron-phonon thermal resistance is given by  $R_{e-ph} = 1/5 \Sigma \Omega T_e^4$ . Inserting these expressions into the expression for  $\tau_1$ , we arrive at

$$\tau_1 = \frac{n \gamma}{5 N_A \Sigma T_e^3}, \quad (5)$$

where  $n = N_e/\Omega$  is the electron density.

We can make a rough estimate of the values of  $\tau_1$  and  $\tau_2$  for the resistive components as follows. For Cr,  $\gamma = 2.9 \text{ mJ mol}^{-1} \text{ K}^{-2}$ .<sup>35</sup> For the transition metals Cu, Cd, Ag and Au,  $n$  lies in the range  $6$  to  $10 \times 10^{28} \text{ m}^{-3}$ .<sup>36</sup> We therefore estimate  $n \approx 5 \times 10^{28} \text{ m}^{-3}$  for CrO. We estimate the value of  $\Sigma$  for both CrO and NbSi to be  $1 \times 10^9 \text{ W m}^{-3} \text{ K}^{-5}$  from measurements made on similar materials (see Table I).

Inserting these values into Eq. 5 we obtain  $\tau_1 \approx 4.8 \times 10^{-8} \text{ K}^3 \text{ s} / T_e^3$  for CrO, which gives, at  $T_e = 33 \text{ mK}$ ,  $\tau_1 \approx 1 \text{ ms}$ ; at  $T_e = 200 \text{ mK}$ ,  $\tau_1 \approx 6 \text{ } \mu\text{s}$ ; and at  $T_e = 500 \text{ mK}$ ,  $\tau_1 \approx 400 \text{ ns}$ . Since these times are all well in excess of pulse lengths which it is feasible to apply with a repetition rate  $100 \text{ MHz} - 1 \text{ GHz}$ , temperature variations on the timescale of the pulsed signal can be neglected.<sup>47</sup>

We now evaluate  $\tau_2$ . According to the Debye model, the lattice specific heat capacity is given by

$$C_{ph} = \frac{12 \pi^4}{5} N_A k_B \left( \frac{T_{ph}}{\theta_D} \right)^3, \quad (6)$$

where  $\theta_D$  is the Debye temperature.<sup>30</sup> The Kapitza thermal boundary resistance is given by  $R_{Kapitza} = 1/\alpha A T_{ph}^3$ . Now since  $\theta_D = \hbar v_s / k_B (6 \pi^2 N_c / \Omega)^{1/3}$ , where  $v_s$  is the velocity of sound, we can use Eq. 6 to write

$$\tau_2 = \frac{2 \pi^2}{5} \frac{k_B^4}{(\hbar v_s)^3} \frac{d}{\alpha}, \quad (7)$$

where  $d$  is the thickness of the resistor. The thickness of the CrO film is  $d = 10 \text{ nm}$  and we take  $v_s$  in CrO to be  $5940 \text{ m s}^{-1}$ .<sup>37</sup> We estimate the value of  $\alpha$  for CrO on SiO<sub>2</sub> to be  $100 \text{ W m}^{-2} \text{ K}^{-4}$  from measurements made on similar metals and substrates (see Table I). Inserting these values into Eq. 7 we obtain  $\tau_2 \approx 60 \text{ ps}$ . Since  $\tau_2$  is much shorter than  $\tau_1$  for all relevant values of  $T_e$ , any changes in  $T_{ph}$  in response to a change in the current passing through the device are for our purposes effectively instantaneous.

### B. Electron temperature

For state-of-the-art parameters for the nanowires (with  $V_c$  up to  $700 \text{ } \mu\text{V}$ ), our measurements and simulations

Article	Material	$\Sigma$ ( $\text{W m}^{-3} \text{K}^{-5}$ )	Material	$\alpha$ ( $\text{W m}^{-2} \text{K}^{-4}$ )
Roukes et al. <sup>31</sup>	Cu	$2 \times 10^9$	Cu-on-sapphire	125
Nahum and Martinis <sup>32</sup>	Cu	$3.7 \times 10^9$		
Verbrugh et al. <sup>33</sup>	Al	$0.2 \text{ to } 0.5 \times 10^9$	Al-on-Si	100
Covington et al. <sup>34</sup>	AuPd	$1.4 \times 10^9$		

TABLE I: Values of the electron-phonon coupling constant  $\Sigma$  and coefficient  $\alpha$  of Kapitza boundary resistance between resistor and substrate from the literature.

indicate that the electron temperature strongly influences the shape of the  $IV$  curve and determines whether it is possible to observe dual Shapiro steps. In this section, we calculate  $T_e$  as a function of the current  $I$  passing through the resistor and use the results to interpret our measurements and simulations.

In thermal equilibrium, the relationship between  $T_e$  and the lattice temperature  $T_{\text{ph}}$  is given by<sup>31</sup>

$$T_e^5 = T_{\text{ph}}^5 + \frac{I^2 R}{\Sigma \Omega}, \quad (8)$$

where  $\Omega$  is the volume of the resistor. Similarly, the relationship between  $T_{\text{ph}}$  and the substrate temperature  $T_0$  is given by<sup>31</sup>

$$T_{\text{ph}}^4 = T_0^4 + \frac{I^2 R}{\alpha A}, \quad (9)$$

where  $A$  is the surface area of the boundary between the resistor and the substrate.

Using these two equations, we plot the dependence of  $T_e$  on the current  $I$  for the CrO resistors used in the measured devices (solid red line in Fig. 16). The result is almost identical over the current range probed if we neglect the temperature difference between the substrate and the lattice. As the current increases from zero to 400 pA (the range used for most of the measurements presented in the previous sections), the electron temperature in the CrO resistors rises from  $T_0$  to 280 mK. Therefore, unlike in our simulations, an entire measured  $IV$  curve is not described by a single electron temperature. Looking again at Fig. 8, we see that, at around 0.65 mV, the curve measured at 33 mK crosses over the simulation at  $T_e = 150$  mK. This is consistent with the experimental  $T_e$  lying below 150 mK for  $V < 0.65$  mV and above 150 mK for  $V > 0.65$  mV. At higher  $T_0$ , the heating due to the applied current is much less pronounced: for  $T_0 = 800$  mK, at 400 pA,  $T_e = 801$  mK; the similarity (see Fig. 8) between the measured and simulated data at this temperature therefore should be expected.

The application of time-varying signals superposed on the dc  $V$  bias leads to additional heating. Taking the additional power dissipation for a continuous-wave ac signal to be  $V_{\text{ac}}^2/2R$ , for a -55-dBm signal (the largest shown in Figs. 4 and 5),  $V_{\text{ac}} = 400$  V and 0.12 pW of additional power is dissipated in addition to the dc power dissipation ( $\sim 0.25$  pW at 32 pA;  $\sim 0.84$  pW at 320 pA).

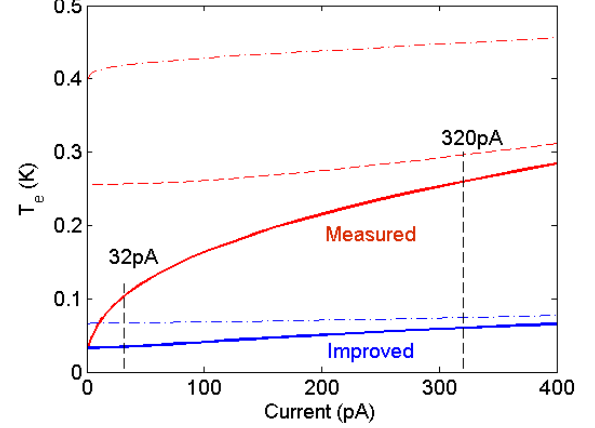


FIG. 16: Electron temperature  $T_e$  as a function of current  $I$  for a single CrO resistor using the dimensions and resistivity of the measured resistors (solid red line). For ac bias frequencies of 100 MHz and 1 GHz, the first dual Shapiro step occurs at 32 pA and 320 pA, respectively (indicated by vertical black dashed lines). The dashed red line includes additional heating from a 400  $\mu\text{V}$  cw signal and the dash-dotted red line includes additional heating from a superimposed 2 mV pulse signal of duration 3 ns and repetition rate 100 MHz. The blue curve illustrates the reduction in  $T_e$  that can be achieved by increasing the volume and resistivity of the CrO resistors (see Table II for the improved parameters). The dash-dotted blue line includes additional heating from a superimposed 5 mV pulse signal of duration 0.1 ns and repetition rate 100 MHz.

The use of a pulsed rather than continuous signal is well-established as an approach to reducing heating. We have shown earlier that the use of pulsed signals is beneficial for obtaining broad steps, and the potentially reduced level of heating in comparison to cw signals is an additional benefit. Within this thermal model (for  $T_{\text{ph}} = T_0$ ) and when the temperature variation of  $\tau_1$  may be neglected, the temperature rise is determined by the average power dissipation during a cycle. Based on the dc  $IV$  characteristics, 400-V pulses of duration 3 ns generate additional power dissipation  $\approx 1$  pW for a 100-MHz repetition frequency, whereas with our improved parameters (see Sec. VIII) much larger 5-mV pulses of duration 0.1 ns generate additional power dissipation  $\approx 0.2$  pW for a 100-MHz repetition frequency or  $\approx 2$  pW for a 1-GHz repetition frequency. The additional temperature rise ex-

pected due to the time-varying signals is also shown in Fig. 16 by a dashed red line (for a 400  $\mu$ V cw ac signal) and by a dash-dotted red line (for a 2 mV pulsed signal).

Figure 16 shows that, at a current of 320 pA, corresponding to the first Shapiro step for a bias frequency of 1 GHz, the electron temperature in the CrO resistors is 260 mK, even with no ac signal applied. Our numerical model suggests that, at these temperatures, the first dual Shapiro step will be washed out. If dual Shapiro steps are to be observed, the electron temperature and therefore the amount of heating need to be reduced.

### VIII. TOWARDS DUAL SHAPIRO STEPS

In Section VII, we introduced a thermal model for the system. Changing the dimensions of the resistive elements and/or their resistivity affects the level of heating. To clarify the dependence of the electron temperature on the dimensions and the resistivity of the resistor, we rewrite Eq. 8 in terms of these quantities, taking  $T_{ph} = T_0$ ,  $P = I^2 R$ ,  $R = \rho l / wd$  and  $\Omega = lwd$ , where  $\rho$  is the resistivity of the CrO film,  $d$  is the film thickness,  $l$  is the length and  $w$  is the width of the resistor,

$$T_e^5 = T_0^5 + \frac{I^2 \rho}{\Sigma (wd)^2}. \quad (10)$$

The electron temperature for a particular current  $I$  is dependent on the resistivity, the width and thickness of the resistor, but independent of the length. Since the overall resistance  $R$  cannot be reduced significantly without affecting the dynamics of the circuit, the best way to reduce  $T_e$  is by increasing  $w$  and  $d$ , while simultaneously also increasing the product  $\rho l$  (to keep  $R$  unchanged). Increasing  $l$  is preferable to increasing  $\rho$ , as  $T_e$  is independent of  $l$ . However, three considerations place upper bounds on  $l$ : (i) very long resistors may be less practical to fabricate, (ii) current leakage to ground via stray capacitance becomes more significant as resistor length increases<sup>27</sup>, and (iii) the resistors must be short in comparison with the wavelength of electromagnetic radiation at GHz frequencies. The stray capacitance of the resistor is also affected by changes to the width and thickness, and this determines the behaviour of the resistor at high frequencies.

The resistivity of the resistors may be modified by changing the material or its composition, for example by increasing the oxygen content of the CrO film (although for larger oxygen contents the resistors become increasingly nonlinear, which is likely to complicate the behaviour of circuits in which they are included.<sup>38</sup>) In Fig. 16, we plot as a solid blue line  $T_e$  as a function of  $I$  for an improved set of properties, detailed in Table II. The resistivity and all three dimensions are increased. We estimate that these changes will increase the total capacitance of each resistor by a factor of 60, and that this will cause a corresponding reduction by a factor of 60 in the roll-off frequency of the impedance. Since the

roll-off frequency of the measured resistors is estimated to be tens of GHz,<sup>26</sup> the roll-off frequency of the larger proposed resistors will still be in the GHz range. With the improved parameters, for a dc current of 320 pA, the current corresponding to the first dual Shapiro step for a bias frequency of 1 GHz, Eq. 10 predicts an electron temperature in the CrO resistors of 61 mK.

	$\rho$ (m $\Omega$ cm)	$d$ (nm)	$w$ (nm)	$l$ ( $\mu$ m)
Measured	0.74	10	80	70
Improved	74	160	2000	280

TABLE II: Parameters of CrO resistors in the measured device, compared with an improved set designed to reduce heating.

Using our improved parameters for the CrO resistors, we repeated our simulation of the  $IV$  curve for the pulsed drive signal of repetition rate 1 GHz and pulse width 0.1 ns (thick lines in Fig. 17), this time including the current dependence of the electron temperature and iterating to obtain self-consistent values for the electron temperature and resulting dc current.

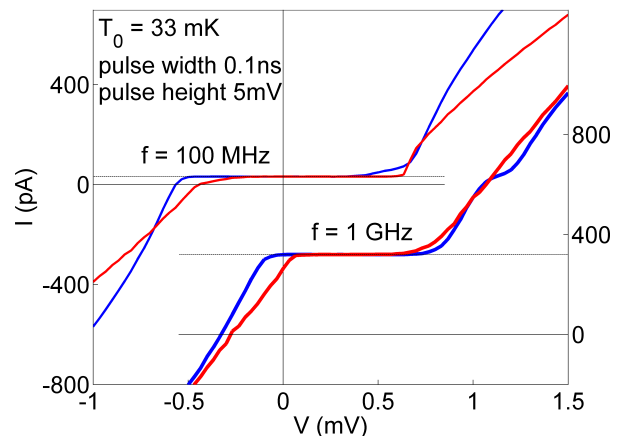


FIG. 17: Simulated  $IV$  curves for a pulsed drive signal of repetition rate 1 GHz (thick lines) or 100 MHz (thin lines), pulse width 0.1 ns and pulse amplitude 5 mV for the parameters corresponding to the measured device (red) and the improved set of parameters (blue). The simulations assume a substrate temperature  $T_0 = 33$  mK and take into account the dependence of the electron temperature  $T_e$  on the current passing through the device. Green dashed lines show the expected currents at which dual Shapiro steps are expected. The step is clearly flatter for the improved parameters.

The shorter pulses result in significantly less heating in the CrO resistors, such that the plateau has sufficient flatness for a prototype current standard, even with the original resistor parameters of the measured device. We

found that the amplitude of the dual Shapiro step generated was maximised by using a higher amplitude of 5 mV for the pulsed drive signal. This step has the satisfactory property of crossing the current axis at zero voltage bias, an ideal property for a current standard.

For a quantum current standard, the current output should exceed 100 pA. At a pulse repetition rate of 1 GHz, the current on the plateau is 320 pA, fulfilling this requirement. At a slower pulse repetition rate of 100 MHz with the same pulse width of 0.1 ns, the breadth of the step is still significant, while the value of the current on the plateau reduced to 32 pA (thin lines in Fig. 17.) In this case, an output current exceeding 100 pA could be achieved with four nanowires in parallel, all driven by the same pulsed signal.

## IX. CONCLUSION

We have presented measurements of the voltage-biased  $IV$  characteristic of a QPSJ circuit consisting of a NbSi nanowire embedded in a resistive environment. The dc  $IV$  characteristic exhibits blockade of the supercurrent and backbending of the transition to the resistive state, both of which are characteristic of coherent transfer of single Cooper pairs. We have also reported the first measurements of the  $IV$  curve with an additional ac voltage bias; we did not find any direct evidence of dual Shapiro steps either for continuous wave or pulsed signals.

We constructed a numerical model of the  $IV$  curve based on QPS, which included the effect of thermal fluctuations via Johnson noise in the series resistors. The simulations were conducted with a fixed electron temperature but nevertheless provided a good qualitative fit to the data and enabled us to predict improved measurement parameters, i.e. a pulsed drive signal with frequency of order 1 GHz and pulse width of order 0.1 ns, to increase the breadth of the dual Shapiro steps and hence their robustness to thermal fluctuations.

In a thermal analysis we considered the time constants of the system and the variation of the electron temperature with current flow in the circuit and infer the presence of significant heating in the measurements. The lack of temperature dependence of the dc  $IV$  characteristic for  $T < 100$  mK, in contrast with the simulation results in

which the dc  $IV$  characteristic remains  $T$ -dependent below 100 mK, gives further evidence that the electron temperature of the device was substantially elevated above the substrate temperature. The result of this heating was sufficient Johnson noise to wash out any dual Shapiro steps.

Following the thermal analysis, we have predicted an improved set of parameters for the series resistors to further reduce heating. The improved parameters would involve resistor composition leading to highly nonohmic properties and the behaviour of circuits containing such resistors requires experimental investigation. Our numerical model predicts that, using these parameters with an increased amplitude for the pulsed drive signal, an observable Shapiro step will be observable even in the presence of the heating due to the drive signal. The step is also predicted to cross the current axis at zero voltage bias, which would be ideal for a prototype QPS-based current standard. In addition we found that, when the repetition rate of the pulsed drive signal is reduced, the breadth of the step may be preserved by preserving the short pulse-duration. The lower repetition rate would have the advantage of reducing heating<sup>27</sup> in the series resistors and several nanowires could be produced in parallel to generate sufficient current for a prototype current standard.

Our conclusion is that, for any future experiments seeking to detect dual Shapiro steps, it will be important to make a number of improvements compared with the experimental set-up which we have described: (i) increasing the dimensions the series resistors, (ii) increasing the resistivity of the resistor material used, (iii) using a pulsed drive signal with a pulse repetition rate of 100 MHz to 1 GHz, (iv) increasing the pulse amplitude, and (v) reducing the pulse width to around 0.1 ns.

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- <sup>39</sup> More extensive tests with CrO-resistor-only samples confirmed that the resistances scale linearly with their dimensions, validating this analysis.
- <sup>40</sup> The NbSi film parameters were measured on stand-alone test wires 20 nm in width.
- <sup>41</sup> The temperature was recorded by a RuO<sub>2</sub> thermometer located at the mixing chamber of the dilution refrigerator.
- <sup>42</sup> We neglect Johnson noise from the NbSi nanowire itself and the  $L_K$  line, as these are in the superconducting state.
- <sup>43</sup> Several attenuators were placed at intervals along the semi-rigid coaxial microwave line in the dilution fridge: 3 dB at 4 K, 10 dB at the 1 K pot, 10 dB between the 1 K pot and the mixing chamber and 1 dB at the mixing chamber. An additional 11 dB of attenuation was present in the line itself and imperfections in the connections (measured by a vector network analyzer). Outside the dilution fridge, an additional 20 dB attenuator was used to reduce the amplitude of the signal leaving the source, which had a range of -20 dBm to 0 dBm.
- <sup>44</sup> For a QPSJ, the  $Q$ -value is given by  $Q = \sqrt{2\pi V_c L_K / 2eR^2}$ .
- <sup>45</sup> Since  $Q \ll 1$ ,  $\omega_c \ll \omega_p$ , where the plasma frequency  $\omega_p = 1/\sqrt{L_K C_{QPS,0}}$ .
- <sup>46</sup> The amplitude values used for the ac simulations do not correspond exactly to those used for the measurements, as the model assumes a simplified version of the circuit.
- <sup>47</sup> Note also that the time step between dc voltage bias points in the  $IV$  curve is much greater than the time constant for the temperature rise, so after the dc voltage bias is changed, the electron temperature reaches thermal equilibrium before the next measurement is made.